WHAT IS CLAIMED IS:

1. A method of providing access to a bus, comprising:

receiving a request for access to the bus;

selecting the request according to a priority associated with the request;

generating a control signal in response to selection of the request;

enabling access to the bus associated with the selected request in response to the control signal.

2. The method of Claim 1, wherein the bus is a PCI bus.

3. The method of Claim 2, wherein the PCI bus operates at a frequency of at least 66 MHZ.

4. The method of Claim 1, wherein the request is received from a device desiring to communicate over the bus.

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5. The method of Claim 1, further comprising:

receiving a plurality of access requests for the bus, each of the plurality of access requests being received from one of a plurality of devices coupled to the bus;

selecting a particular one of the plurality of access requests according to a predetermined priority protocol;

generating a control signal corresponding to the selected particular one of the plurality of access requests;

providing the control signal to a particular one of the plurality of devices that sent the selected particular one of the plurality of access requests, the control signal enabling the particular one of the plurality of devices to access the bus.

6. The method of Claim 5, further comprising:

selecting a next one of the plurality of access requests according to the predetermined priority protocol;

generating a control signal corresponding to the selected next one of the plurality of access requests;

providing the control signal to a next one of the plurality of devices that sent the selected next one of the plurality of access requests, the control signal enabling the next one of the plurality of devices to access the bus prior to an end of access to the bus for the particular one of the plurality of devices.

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7. The method of Claim 6, further comprising:

determining an end of access to the bus for the particular one of the plurality of devices;

initiating access to the bus by the next one of the plurality of devices in response to the end of access to the bus for the particular one of the plurality of devices.

8. The method of Claim 7, further comprising:

generating a disabling control signal in response to the end of access to the bus for the particular one of the plurality of devices;

preventing the particular one of the plurality of devices from accessing the bus in response to the disabling control signal.

9. The method of Claim 1, further comprising:

limiting a number of generated control signals in order to control a load on the bus.

10. The method of Claim 1, further comprising:

generating a disable control signal for a request not selected in order to disable access to the bus.

11. A system for providing access to a bus, comprising:

a bus controller;

a plurality of processing devices coupled to the bus controller by a bus;

a plurality of enabling switches on the bus, each enabling switch coupled to a corresponding processing device, each enabling switch providing access to the bus for its corresponding processing device in response to a control signal from the bus controller.

12. The system of Claim 11, wherein the bus controller allows simultaneous access to the bus by a predetermined number of the plurality of processing devices in order to limit a load on the bus.

13. The system of Claim 11, wherein the bus controller receives a plurality of access requests from the plurality of processing devices for access to the bus.

14. The system of Claim 13, Wherein the bus controller arbitrates the plurality of access requests from the plurality of processing devices according to a predetermined protocol.

15. The system of Claim 11, wherein the bus is a PCI bus.

16. The system of Claim 15, wherein the PCI bus operates at a frequency of approximately 66 MHZ.

17. A PCI bus, comprising:

a plurality of pass transistors, each pass transistor operable to provide bus access for an associated processing device, each pass transistor operable to receive a control signal to enable and disable bus access for its associated processing device.

18. The PCI bus of Claim 17, wherein a particular pass transistor receives an enable control signal in response to an access request sent by its associated processing device.

19. The PCI bus of Claim 17, wherein a particular pass transistor is operable to disable bus access for its associated processing device such that the particular processing device does not appear to be coupled to the PCI bus.

20. The PCI bus of Claim 17, wherein each of the processing devices is operable to communicate at a 66 MHZ rate.